AMENDMENTS TO THE CLAIMS

Please enter the following amendments:

1. (Currently Amended) A semiconductor memory device comprising:

a plurality of memory cells arranged in a matrix; and

a gate line, a word line, a bit line to be selected based on an address signal and to supply a writing voltage to the memory cell to be written, and a source line to which a power supply potential is supplied, wherein

each of said plurality of memory cells includes:

a storage transistor having a first impurity region and a second impurity diffusion region opposed to each other through a first channel formation region, a first gate electrode formed above said first channel formation region, and a charge accumulation node formed below said first channel formation region; and

an access transistor connected to said storage transistor in series, having said first impurity diffusion region, a third impurity diffusion region opposed to said first impurity diffusion region through a second channel formation region, and a second gate electrode formed above said second channel formation region,

said second impurity diffusion region is connected to said source line, said third impurity diffusion region is connected to said bit line, said first gate electrode is connected to said gate line, and said second gate electrode is connected to said word line, and

by turning on/off said access transistor, a potential of said first impurity diffusion region is switched to a fixed potential or a floating state, to thereby control the potential of said charge

accumulation node, and a threshold voltage of said storage transistor is thereby set at high level or low level.

2. (Previously Presented) The semiconductor memory device according to claim 1, wherein

said threshold voltage of said storage transistor is set at high level by raising a potential of said first gate electrode to high level from low level, with said access transistor turned on, and

said threshold voltage of said storage transistor is set at low level, by raising the potential of said first gate electrode to high level from low level, with said access transistor turned off.

3. (Previously Presented) The semiconductor memory device according to claim 1, further comprising:

an SOI substrate in which a semiconductor substrate, an insulating layer, and a semiconductor layer are laminated in this order, wherein

said first to third impurity diffusion regions and said first and second channel formation regions are respectively formed in said semiconductor layer, and

said charge accumulation node is constituted as a part of said semiconductor layer.

4. (Withdrawn) The semiconductor memory device according to claim 1, further comprising:

a substrate on which a semiconductor substrate of a first conductive type, a first well of a second conductive type, and a second well of said first conductive type are laminated in this order, wherein

said first to third impurity diffusion regions and said first and second channel formation regions are respectively formed in an upper surface of said second well, and

said charge accumulation node is constituted as a part of said second well.

5. (Previously Presented) The semiconductor memory device according to claim 1, further comprising:

a first memory cell in which said threshold voltage of said storage transistor is set at high level;

a first reference bit line connected to said first memory cell;

a second memory cell in which said threshold voltage of said storage transistor is set at low level;

a second reference bit line connected to said second memory cell; and

a sense amplifier circuit that compares each potential of said first and second reference bit lines and the potential of the bit line connected to a reading memory cell serving as a reading object, and thereby detects whether said threshold voltage of said storage transistor provided in said reading memory cell is set at high level or low level.

6. (Previously Presented) The semiconductor memory device according to claim 5, wherein

said storage transistor, said access transistor, a first transistor, and a second transistor are sequentially connected in series from a power supply potential side, between said power supply potential and a ground potential, and

each gate of said first and second transistors is connected to a drain of said first transistor.

7. (Previously Presented) The semiconductor memory device according to claim 1, wherein

when said threshold voltage of said storage transistor provided in a writing memory cell serving as a writing object is set at high level, the potential of low level is applied to a bit line connected to said writing memory cell, and when said threshold voltage of said storage transistor provided in said writing memory cell is set at low level, a writing circuit for applying the potential of high level to said bit line connected to said writing memory cell is further provided.

8. (Previously Presented) The semiconductor memory device according to claim 1, further comprising:

an SOI substrate in which a semiconductor substrate, an insulating layer, and a semiconductor layer are laminated in this order, wherein

said SOI substrate includes a memory cell array region formed with said plurality of memory cells, and a peripheral circuit region formed with a peripheral circuit,

a first element isolation film having a bottom face that is brought into contact with an upper surface of said insulating layer is formed in said memory cell array region, and

a second element isolation film having the bottom face that is not brought into contact with the upper surface of said insulating layer is formed in said peripheral circuit region.

9 – 10. (Canceled)